What is claimed is:

1. A method of making a multiple gate electrode on a semiconductor device, comprising the steps of:

coating a layer of gate electrode material over a semiconductor device that has been previously coated with a thin film of gate dielectric; and

planarizing the layer of gate electrode material to a substantially planar surface prior to patterning the gate electrode material to form a discrete multiple gate electrode on the semiconductor device.

2. The method of claim 1, further comprising the steps of:

applying a photoresist mask of substantially uniform thickness on the planar top surface of the planarized gate electrode material;

patterning the photoresist mask to cover a corresponding pattern of the discrete multiple gate electrode; and

etching the gate electrode material that is uncovered by the photoresist mask to form the discrete multiple gate electrode.

3. The method of Claim 1, further comprising the step of:

conforming the layer of gate electrode material with a step height increase corresponding to an increased step height of the semiconductor device.

4. The method of claim 1 wherein, the semiconductor device comprises a silicon fin.

5. The method of claim 1 wherein, the semiconductor device comprises a fin of silicon and germanium.

6
5. The method of claim 1, further comprising the steps of:

applying a photoresist mask of substantially uniform thickness on the planar top surface of the planarized gate electrode material, the mask comprising photoresist and a mask material selected from the group comprising, silicon nitride, silicon oxynitride, silicon oxide and photo resist, or combinations thereof;

patterning the photoresist mask to cover a corresponding pattern of the multiple gate electrode; and

etching the gate electrode material that is uncovered by the photoresist mask to form the discrete multiple gate electrode.

7
6. The method of claim 1, further comprising the steps of:

applying a photoresist mask of substantially uniform thickness on the planar top surface of the planarized gate electrode material;

patterning the photoresist mask to cover a corresponding pattern of the multiple gate electrode; and

plasma etching the gate electrode material that is uncovered by the photoresist mask to form the patterned multiple gate electrode.

8
7. The method as recited in claim 1, further comprising the step of: applying a mask over the planarized surface, wherein the mask is of substantially uniform thickness for accurate patterning thereof.

9
8. The method of claim 1 wherein, the gate dielectric comprises silicon oxide.

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9. The method of claim 1 wherein, the gate dielectric comprises silicon oxynitride.

11
10. The method of claim 1 wherein, the gate dielectric comprises a high permittivity material.

12
11. The method of claim 1 wherein, the gate dielectric comprises a material having a permittivity greater than 5.

13
12. The method of claim 1 wherein, the gate dielectric comprises a thickness in the range of 3 and 100 Angstroms.

14
13. The method of claim 1 wherein, the multiple gate electrode comprises polycrystalline silicon.

15
14. The method of claim 1 wherein, the multiple gate electrode comprises a conductive material.

16
15. The method of claim 1 wherein, the multiple gate electrode comprises a metal material.

17
16. A semiconductor device having a multiple gate electrode, comprising:

the semiconductor device having a projecting fin;

a multiple gate electrode on more than one side of the fin, the multiple gate electrode having a substantially planar surface extending over the fin; and

a patterned mask on the planar surface of the multiple gate electrode, the patterned mask having a substantially uniform thickness and a substantially planar surface.

18
17. The semiconductor device of claim 17 wherein, the multiple gate electrode is a portion of a layer of gate electrode material having a planarized surface, and the planarized surface includes the planar surface of the multiple gate electrode.